WAFER-BASED ION TRAPS

ABSTRACT OF THE DISCLOSURE

An apparatus for an ion trap includes a semiconductor or dielectric wafer with front and back surfaces, a sequence of alternating conductive and dielectric layers formed over said front surface, and a bottom conductive layer. The sequence includes top and middle conductive layers, wherein the middle conductive layer is closer to the wafer than the top conductive layer. The middle conductive layer includes a substantially right cylindrical cavity that crosses a width of the middle conductive layer. The top and bottom conductive layers cap respective first and second ends of the cavity. The top conductive layer includes a hole that forms a first access port to the cavity. The wafer includes via through the width of the wafer. The via provides another access to the cavity via the back surface of the wafer. The wafer is substantially thicker than the sequence of layers.